Amendments to the Specification:

Please replace the original paragraph [0017] with the following amended paragraph:

[0017] When an interrupt occurs, a CPU of the microprocessor (e.g., the interrupt processing unit 34 of the microprocessor 30) pushes a current program counter address and a bank number of the current memory bank onto a stack 36 in that order, and then switches the working memory bank to bank 0 of the external memory 22 to execute the interrupt service routine by setting the memory bank selector 32 to the bank number of the memory bank storing the interrupt service routine. When finished executing the interrupt service routine, the CPU (e.g., the interrupt processing unit 34) pops the bank number of the memory bank and the program counter address from the stack 36 in that order, and switches the microprocessor back to the memory bank [[and]] to continue executing the interrupted program by restoring the popped bank number to the memory bank selector 32 for selecting the memory bank corresponding to the popped bank number.